US-PAT-NO: 5375082

DOCUMENT-IDENTIFIER: US 5375082 A

TITLE: Integrated, nonvolatile, high-speed analog random access memory

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Brief Summary Text - BSTX (18):
Coleman (U.S. Pat. No. 4,831,427)--This memory uses a transistor structure where the gate is ferromagnetic in place of standard conductors. As will be seen from the discussion of the present invention which follows, this is completely different from the structure of this invention where transistors which are standard CMOS implementations in tandem are used with an **analog memory cell**.

Brief Summary Text - BSTX (22):
Accordingly, it is an object of this invention to provide an **analog memory cell** which is viable to use commercially.

Brief Summary Text - BSTX (23):
It is another object of this invention to provide an **analog memory cell** which can be integrated into standard CMOS technology or the like.

Brief Summary Text - BSTX (24):
It is still another object of this invention to provide a method for operating and energizing an **analog memory cell** which provides for sure and repeatable setting of the memory cell at its discrete levels of operation.

Brief Summary Text - BSTX (25):
It is yet another object of this invention to provide an **analog memory cell** which can be formed of materials which will withstand space operations and similar harsh environments without malfunctioning.

Claims Text - CLTX (1):
1. An **analog memory cell** for storing analog data, and reading out said analog data with an electronic readout circuit, the **analog memory cell** comprising:

Claims Text - CLTX (8):
2. The **analog memory cell** of claim 1 wherein:

Claims Text - CLTX (11):
3. The **analog memory cell** of claim 1 wherein:

Claims Text - CLTX (13):
4. The **analog memory cell** of claim 1 wherein:

Claims Text - CLTX (15):
5. The **analog memory cell** of claim 1 and additionally comprising:

Claims Text - CLTX (17):
6. The **analog memory cell** of claim 5 wherein:

Claims Text - CLTX (19):
7. The **analog memory cell** of claim 5 wherein:

Claims Text - CLTX (21):
8. The **analog memory cell** of claim 7 wherein:

Claims Text - CLTX (23):
9. The **analog memory cell** of claim 1 and additionally comprising:

Claims Text - CLTX (25):
10. The **analog memory cell** of claim 9 and additionally comprising:

Claims Text - CLTX (27):
11. The **analog memory cell** of claim 1 wherein:

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("5360981").PN.	US-PGPUB; USPAT	OR	OFF	2005/06/30 09:27
L2	1897	analog adj memory	US-PGPUB; USPAT	OR	ON	2005/06/30 09:27
L3	424	analog adj memory adj (device or cell)	US-PGPUB; USPAT	OR	ON	2005/06/30 09:27
L4	374	3 and (electrode or gate)	US-PGPUB; USPAT	OR	ON	2005/06/30 09:28
L5	255	4 and @ad<"20001208"	US-PGPUB; USPAT	OR	ON	2005/06/30 09:28